



# Samsung SDS Nexplant<sup>SLM</sup>

## An E2E Simulation Lifecycle Management solution that utilizes data driven design for business innovation

Up till now, the product design and verification field was too reliant on Point Tools such as CAD/CAE/in-house solutions as well as the individual capabilities of engineers, and was thus unable to respond to market requirements for product complexity and process refinement. That is why it is now necessary to automate and optimize CAE tasks utilizing data driven design through ICT technology-based platforms such as BDA and AI.

### Execution environment capable of quickly responding to change

Provides easy-to-use automation environment with workflow-based toolchain configuration

Provides EDA tool execution environment utilizing scenario-based verification script

\*EDA : Electronic Design Automation  
\*HPC : High Performance Computing

### Big data platform optimized for CAE

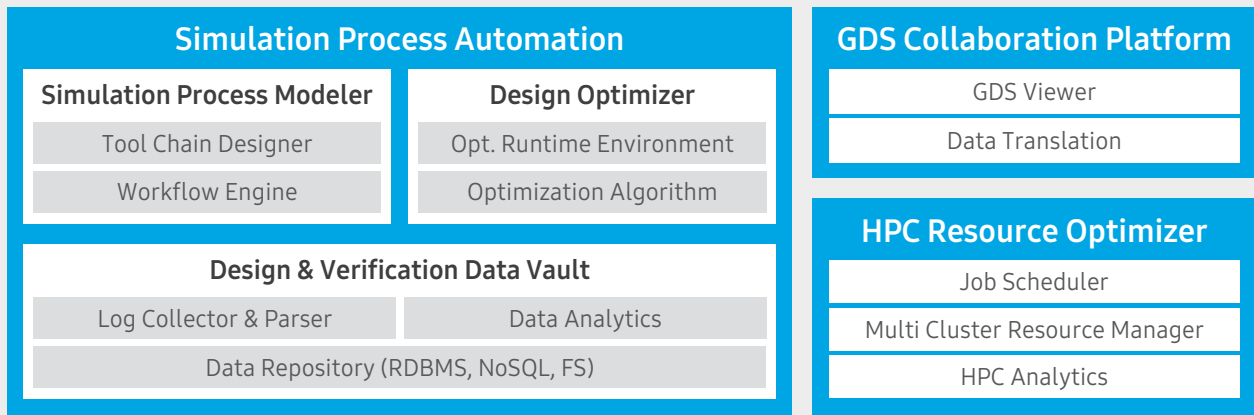
Collects and processes data by automatically searching complexly structured files generated in CAE Computing Farm (HPC)

Extracts meaningful data from large-scale layout data and visualizes in real-time

### Hardware resource optimization for mixed workloads

Provides a sharable environment with a single resource pool for various workloads including HPC, BDA, and AI

Predicts hardware resource demand/failure based on analytics, and optimizes job scheduling including optimized job parameter estimation



■ Offering items

## Features

### Simulation Process Automation

Toolchain automation  
 Optimized design runtime framework & provision of verified algorithm  
 CAE log scanner, real-time parser & verification dashboard

### GDS Collaboration Platform

Provision of GDS data platform and viewer  
 Defect identification and equipment recipe automation through comparison/analysis between design(GDS) – Real(SEM)

### HPC Resource Optimizer

HPC asset optimization I  
 Intelligent job scheduler-based analysis

## Benefits

Increases productivity by reducing time required for design (for semiconductor design, 30% shorter timing closure L/T)

Boosts product quality and reduces quality issues in the manufacturing process(20% improvement of fan blade performance, 40% decrease in mold flash, 80% decrease in mold deformation)

Detects product verification status/results in real-time and eliminates non-value adding activities (75% decrease in time for ASIC verification status and result)

Secures a real-time collaboration environment of more than 200GB of GDS data (similar to Google Map's UI)

Ensures the automation of in-line defect identification based on thousands of pieces of inspection/measurement information

Secures unmanned setup of inspection/measurement equipment based on design data

Optimizes HPC resource usage (90% of hardware's operation capacity)& minimizes job delays

## Contact Us



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